CLAIM AMENDMENTS

1-5. (Canceled)

6. (Currently Amended) A microprocessor for executing instructions, comprising:

a timing and control unit ~~for retrieving~~ configured to:

retrieve an instruction to compose a plurality of processes running in parallel from a memory, the instruction being expressed in a reflective process algebra, the reflective process algebra being arranged to represent a name as a literalization of a process and a process as a deliteralization of a name,

~~decoding~~ decode the instruction,

~~fetching~~ fetch data connected with the instruction, the data comprising at least a first name that is a literalization of a first process and a second name that is a literalization of a second process, the first name and the second name being obtained using the reflective process algebra,

compose the plurality of processes running in parallel; and

~~saving the~~ literalize a result of the composing, including saving the result of the composing ~~the data including names obtained by literalizing processes in a reflective process algebra~~; and

an arithmetic and logic unit ~~for performing an operation specified by the instruction~~ configured to perform the composing of the plurality of processes running in parallel, the composing including deliteralizing the first name and the second name; ~~the instruction being expressed in a reflective process algebra, the reflective process algebra being capable of representing names as literalization of processes and~~

~~processes as deliteralization of names~~

wherein a synchronization of the microprocessor includes a compiler-created explicit synchronization model based on the reflective process algebra.

7. (Original) The microprocessor of Claim 6, further comprising a register array for storing the result of the executed instruction.

8. (Original) The microprocessor of Claim 7, further comprising an instruction register and decoder for holding the instruction of the microprocessor is executing.

9. (Original) The microprocessor of Claim 8, further comprising bus connections for allowing the microprocessor to receive data into memory internally and for communicating result of the executed instruction externally.

10. (Original) The microprocessor of Claim 9, wherein the timing and control unit, the arithmetic and logic unit, and the instruction register and decoder communicates via ports that have unilateral contracts associated with ports.

11-44. (Canceled)

45. (Currently Amended) An array of microprocessors for executing instructions, comprising:

at least one microprocessor that includes one or more components that are synchronized based on a program compiler configured to compile a program written in a reflective process algebra, the reflective process algebra being arranged to represent a name as a literalization of a process and a process as a deliteralization of a name:

a timing and control unit for retrieving an instruction from a memory, decoding the instruction, fetching data connected with the instruction, and literalizing a result of a composing of a plurality of processes in parallel, including saving the result of the composing, the data including names obtained by literalizing processes in the reflective process algebra; and

an arithmetic and logic unit ~~for performing an operation specified by the instruction, the instruction being expressed in a reflective process algebra, the reflective process algebra being capable of representing names as literalization of processes and processes as deliteralization of names~~ configured to perform the composing of the plurality of processes running in parallel, the composing including deliteralizing the names obtained by the literalizing process.

46. (Original) The array of microprocessors of Claim 45, wherein the array of microprocessors are on a single integrated circuit.

47. (Original) The array of microprocessors of Claim 45, wherein the array of microprocessors are on multiple integrated circuits, the multiple integrated circuits being mounted on a single board.

48. (Original) The array of microprocessors of Claim 45, wherein the array of microprocessors are on multiple integrated circuits, the multiple integrated circuits being mounted on multiple boards, the multiple boards being housed on a single rack of a computer.

49. (Original) The array of microprocessors of Claim 45, wherein the array of microprocessors are on multiple integrated circuits, the multiple integrated circuits being mounted on multiple boards, the multiple boards being housed on multiple racks of multiple computers.

50. (Original) The array of microprocessors of Claim 45, further comprising a network for coupling one or more microprocessors, the network being selected from a group consisting of permanent connections and temporary connections.

51. (Original) The array of microprocessors of Claim 45, wherein the components of the at least one microprocessor are synchronized by instructions produced by a compiler that compiles a program written in the reflective process algebra.

52. (Original) The array of microprocessors of Claim 45, wherein the array of microprocessors are synchronized by instructions produced by a compiler that compiles a program written in the reflective process algebra.

53. (Original) The array of microprocessors of Claim 45, wherein the components of the at least one microprocessor lacks circuitry for predicting a next instruction to be executed.